The stamp of the USPTO, placed hereon, acknowledges receipt of:

Applicant: Sheu, et al.

Docket No.:

TSM03-0140

Serial No:

10/619,828

Art Unit:

2829

Filed:

July 15, 2003

Date Mailed: June 23, 2005

TITLE:

Self-Aligned MOSFET having an Oxide Region below the Channel

Certificate of Mailing via First Class Mail (1 page) Information Disclosure Statement (1 original & 1 copy = 2 pages) IDS Form PTO/SB/08b (1 page) citing 2 references Copies of (2) references Return Postcard

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Docket No.:

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July 15, 2003

Examiner:

Dana Farahani

For:

Self-Aligned MOSFET having an Oxide Region below the Channel

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants wish to bring to the attention of the U.S. Patent and Trademark Office the information noted on the enclosed PTO Form PTO/SB/08b, which may be considered material to the examination of the above-identified application.

This Information Disclosure Statement is submitted under 37 C.F.R. §1.97(c) together with a \$180.00 fee under 37 C.F.R. §1.17(p) after the C.F.R. §1.97(b) time period, but before final action or notice of allowance, whichever occurs first.

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Respectfully submitted,

June 23, 2005

Steven H. Slater

Attorney for Applicants

Reg. No. 35,361

Slater & Matsil, L.L.P. 17950 Preston Road. Suite 1000

Dallas, Texas 75252 Tel: (972) 732-1001

Fax: (972) 732-9218

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Ä	Substitute for total 1449B/PEO RADE STATEMENT BY APPLICANT				Complete if Known		
1	v .	. Gar	ADEM		Application Number	10/619,828	
i	TRADA	TFORMATION	N DISCLOSI	JRE	Filing Date	07/15/2003	
	s	TATEMENT I	MENT BY APPLICANT		First Named Inventor	Sheu, et al.	
					Art Unit	2829	
		(Use as many sh	eets as necessary)		Examiner Name	Dana Farahani	
	Sheet	1	of	1	Attorney Docket Number	TSM03-0140	

NON PATENT LITERATURE DOCUMENTS								
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²					
	1	WOLF, S., et al., "Silicon Processing For The VLSI Era," Volume 1: Process Technology, Second Edition, Lattice Press, Sunset Beach, California, 2000, pp. 834-835.						
	2	WOLF, S., "Silicon Processing For The VLSI Era," Volume 2: Process Integration, Lattice Press, Sunset Beach, California, 1990, pp. 144-145.						

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Examiner	Date	
Signature	Considered	
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Respectfully submitted,

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